INNOLUX DISPLAY CORPORATION

LCD MODULE

APPLICATION NOTE

Customer:	**ALL**
LCD SIZE:	**7.0D**
Date:	**2009/8/10**
Version:	**C**

Remark
■**Without PCB**

Approved by	Reviewed by	Prepared by
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Record of Revision

Version	Revise Date	Page	Content
A	2009/3/01		Initial Release
B	2009/7/10		Modify Recommend LED Driver
C	2009/8/10		Add Model

1. Module Introduction

1.1 Module Photo

Model	Module photo	
	Top side	Bottom side
AT070TN92 AT070TN93 AT070TN94		

1.2 Module Comparison Table

Module name	Brightness(nits)	Pin Num.	Recommended connector
AT070TN92	250(without TP)	50 pin	FH12A-50S-0.5SH
AT070TN93	320(with TP)	50pin	FH12A-50S-0.5SH
AT070TN94	400(without TP)	50 pin	FH12A-50S-0.5SH

2. Pin Assignment Table

Pin No.	AT070TN92 &AT070TN94			
	Symbol			
Pin No.	Symbol	I/O	Function	Remark
1	V_{LED+}	P	Power for LED backlight (Anode)	
2	V_{LED+}	P	Power for LED backlight (Anode)	
3	V_{LED-}	P	Power for LED backlight (Cathode)	
4	V_{LED-}	P	Power for LED backlight (Cathode)	
5	GND	P	Power ground	
6	V_{COM}	I	Common voltage	
7	DV_{DD}	P	Power for Digital Circuit	
8	MODE	I	DE/SYNC mode select	Note 1
9	DE	I	Data Input Enable	
10	VS	I	Vertical Sync Input	
11	HS	I	Horizontal Sync Input	
12	B7	I	Blue data(MSB)	
13	B6	I	Blue data	
14	B5	I	Blue data	
15	B4	I	Blue data	
16	B3	I	Blue data	
17	B2	I	Blue data	
18	B1	I	Blue data	Note 2
19	B0	I	Blue data(LSB)	Note 2
20	G7	I	Green data(MSB)	
21	G6	I	Green data	
22	G5	I	Green data	
23	G4	I	Green data	
24	G3	I	Green data	
25	G2	I	Green data	
26	G1	I	Green data	Note 2
27	G0	I	Green data(LSB)	Note 2
28	R7	I	Red data(MSB)	
29	R6	I	Red data	

30	R5	I	Red data	
31	R4	I	Red data	
32	R3	I	Red data	
33	R2	I	Red data	
34	R1	I	Red data	Note 2
35	R0	I	Red data(LSB)	Note 2
36	GND	P	Power Ground	
37	DCLK	I	Sample clock	Note 3
38	GND	P	Power Ground	
39	L/R	I	Left / right selection	Note 4
40	U/D	I	Up/down selection	Note 4
41	V_{GH}	P	Gate ON Voltage	
42	V_{GL}	P	Gate OFF Voltage	
43	AV_{DD}	P	Power for Analog Circuit	
44	RESET	I	Global reset pin.	Noet5
45	NC	-	No connection	
46	V_{COM}	I	Common Voltage	
47	DITHB	I	Dithering function	Noet6
48	GND	P	Power Ground	
49	NC	-	No connection	
50	NC	-	No connection	

I: input, O: output, P: Power

Note 1: DE/SYNC mode select. Normally pull high.
When select DE mode, MODE="1", VS and HS must pull high.
When select SYNC mode, MODE="0", DE must be grounded.

Note 2: When input 18 bits RGB data, the two low bits of R,G and B data must be grounded

Note 3: Data shall be latched at the falling edge of DCLK.

Note 4: Selection of scanning mode

Setting of scan control input		Scanning direction
U/D	L/R	
GND	DV_{DD}	Up to down, left to right
DV_{DD}	GND	Down to up, right to left
GND	GND	Up to down, right to left
DV_{DD}	DV_{DD}	Down to up, left to right

Note 5: Global reset pin. Active low to enter reset state. Suggest to connect with an RC reset circuit for stability. Normally pull high

Note 6: Dithering function enable control, normally pull high.
When RGB is 6 bit DITHB="1",Disable internal dithering function,
When RGB is 8 bit DITHB="0",Enable internal dithering function,

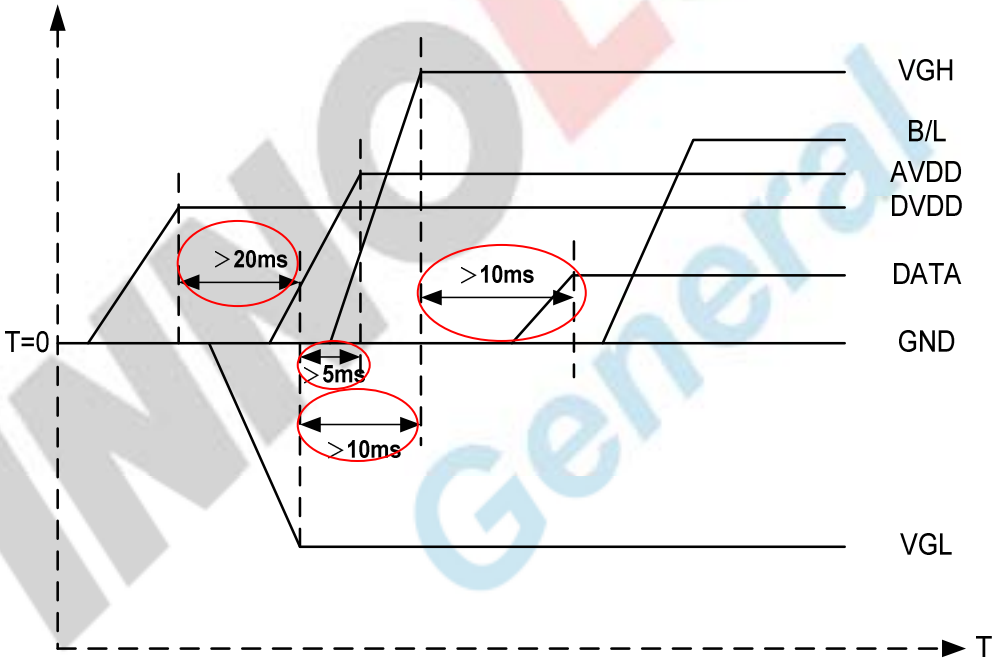
3. Power &Timing Characteristic

3.1. Power Sequence

Customer should follow our product power sequence, other it would lead to display abnormal, please refer to the figures as below.

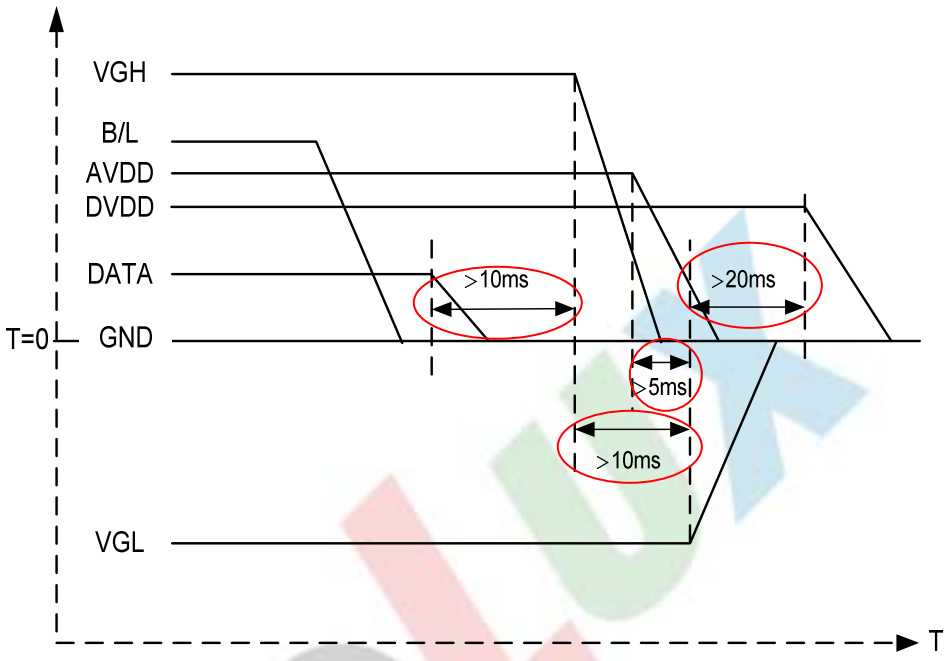
3.1.1 AT070TN92 & AT070TN94

Power On:



DV_{DD}→VGL→VGH→Data→B/L

Power Off :



B/L→Data→VGH→VGL→DV_{DD}

Note: Data include R0~R7, B0~B7, GO~G7, U/D, L/R, DCLK, HS,VS,DE.

3.2 Power Operation Conditions

Customer should notice the red mark specially, if you do not follow it, it would lead to display abnormal.

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Power voltage	DV_{DD}	3.0	3.3	3.6	V	Note 2
	AV_{DD}	10.2	10.4	10.6	V	
	V_{GH}	15.3	16.0	16.7	V	
	V_{GL}	-7.7	-7.0	-6.3	V	
Input signal voltage	V_{COM}	3.8	4.0	4.2	V	
Input logic high voltage	V_{IH}	0.7 DV_{DD}	-	DV_{DD}	V	Note 3
Input logic low voltage	V_{IL}	0	-	0.3 DV_{DD}	V	

Note 1: Be sure to apply DV_{DD} and V_{GL} to the LCD first, and then apply V_{GH}.

Note 2: DV_{DD} setting should match the signals output voltage (refer to Note 3) of customer's system board.

Note 3: DCLK,HS,VS,RESET,U/D, L/R,DE,R0~R7,G0~G7,B0~B7,MODE,DITHB.

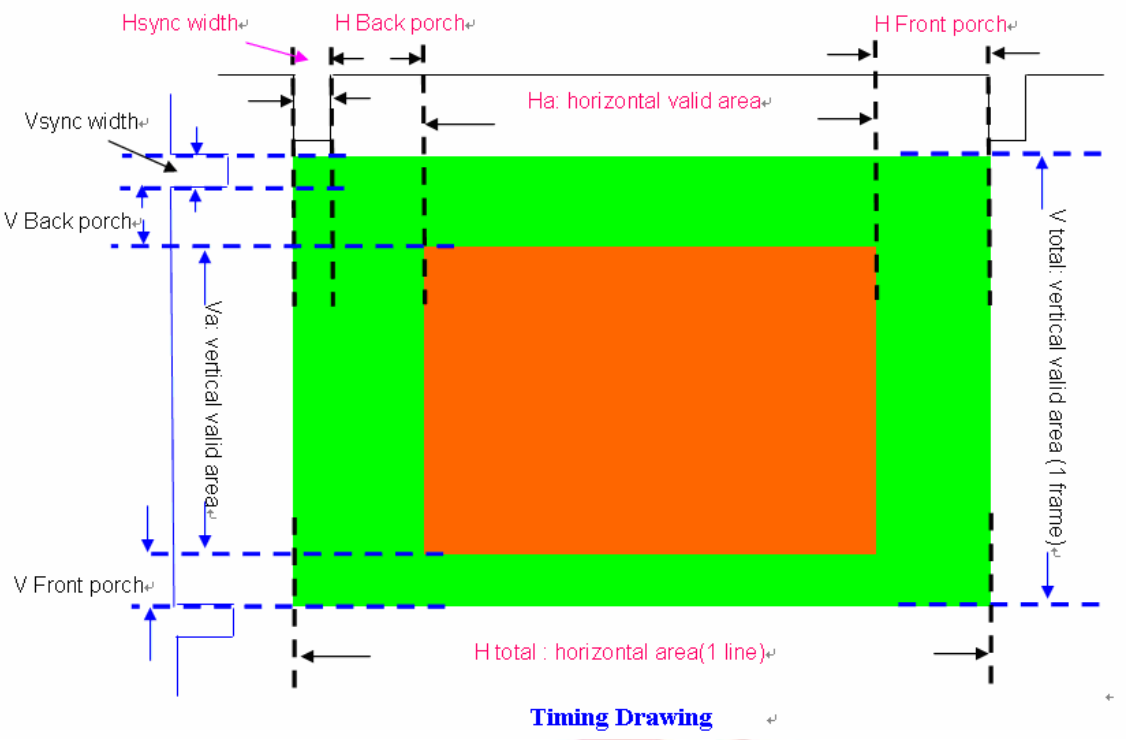
3.3 Timing Description

Input signals must follow our timing specification, Otherwise the LCM will display abnormally.

About the detail timing parameters of LCD display, please follow the product specification.

3.3.1AC Electrical Characteristics

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
HS setup time	Thst	8	-	-	ns	
HS hold time	Thhd	8	-	-	ns	
VS setup time	Tvst	8	-	-	ns	
VS hold time	Tvhd	8	-	-	ns	
Data setup time	Tdsu	8	-	-	ns	
Data hole time	Tdhd	8	-	-	ns	
DE setup time	Tesu	8	-	-	ns	
DE hole time	Tehd	8	-	-	ns	
DV_{DD} Power On Slew rate	TPOR	-	-	20	ms	From 0 to 90% DV_{DD}
RESET pulse width	TRst	1	-	-	ms	
DCLK cycle time	Tcoh	20	-	-	ns	
DCLK pulse duty	Tcwh	40	50	60	%	



Timing Drawing

Timing Formula:

DCLK = (Hw + Hbp + Ha +Hfp)*(Vw + Vbp + Va +Vfp)*Fvsync (Unit : Hz)

Fhsync = (Vw+ Vbp + Va +Vfp)*Fvsync (Unit : Hz)

Remark:

1. Fhsync is Hsync frequency, and Fvsync is Vsync frequency.
2. Parameter Table.

Parameter	Description	Unit
Hw	Hsync Width	DCLK
Hbp	Horizontal back porch	DCLK
Ha	Horizontal valid area	DCLK
Hfp	Horizontal front porch	DCLK
Vw	Vsync Width	Hsync(Line)
Vbp	Vertical back porch	Hsync(Line)
Va	Vertical valid area	Hsync(Line)
Vfp	Vertical front porch	Hsync(Line)
DCLK	Dot clock	Hz

3.3.2Timing Chart

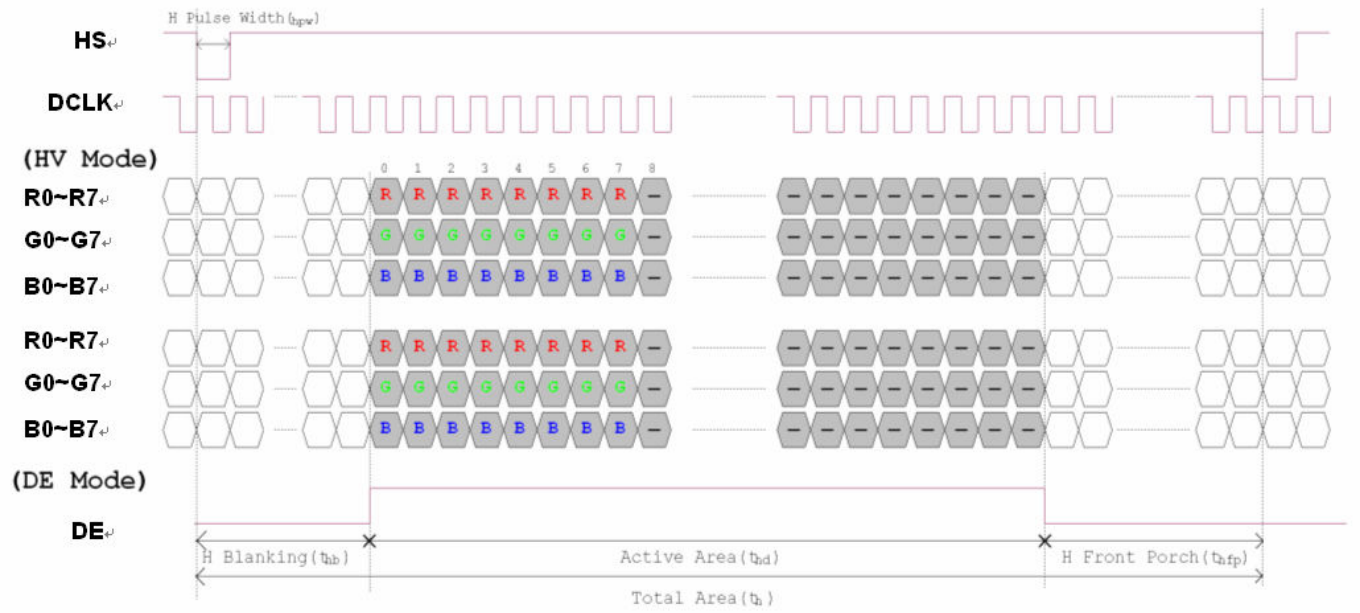


Figure 3. 1 Horizontal input timing diagram.

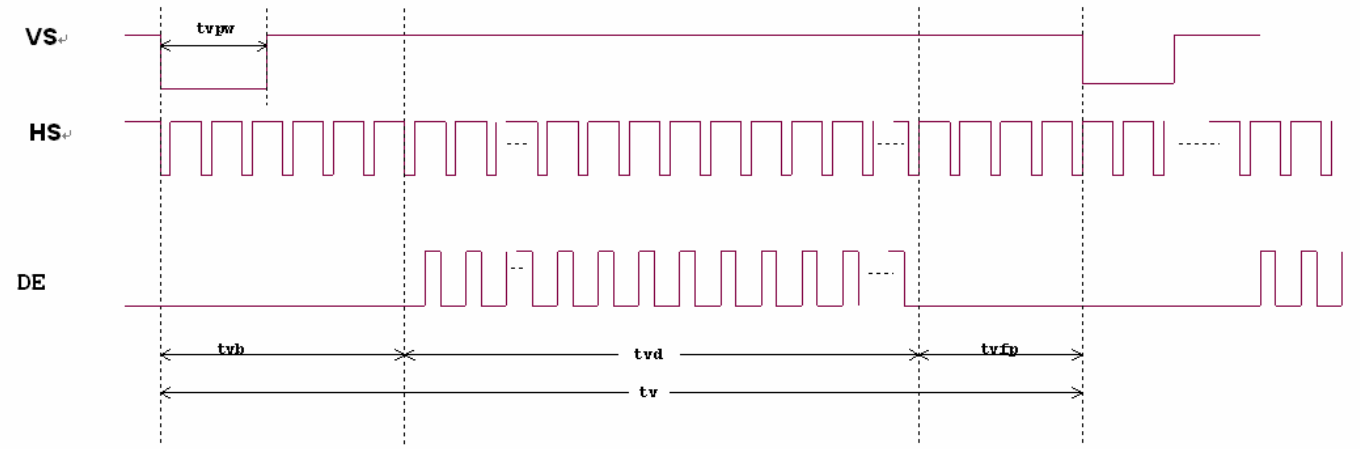


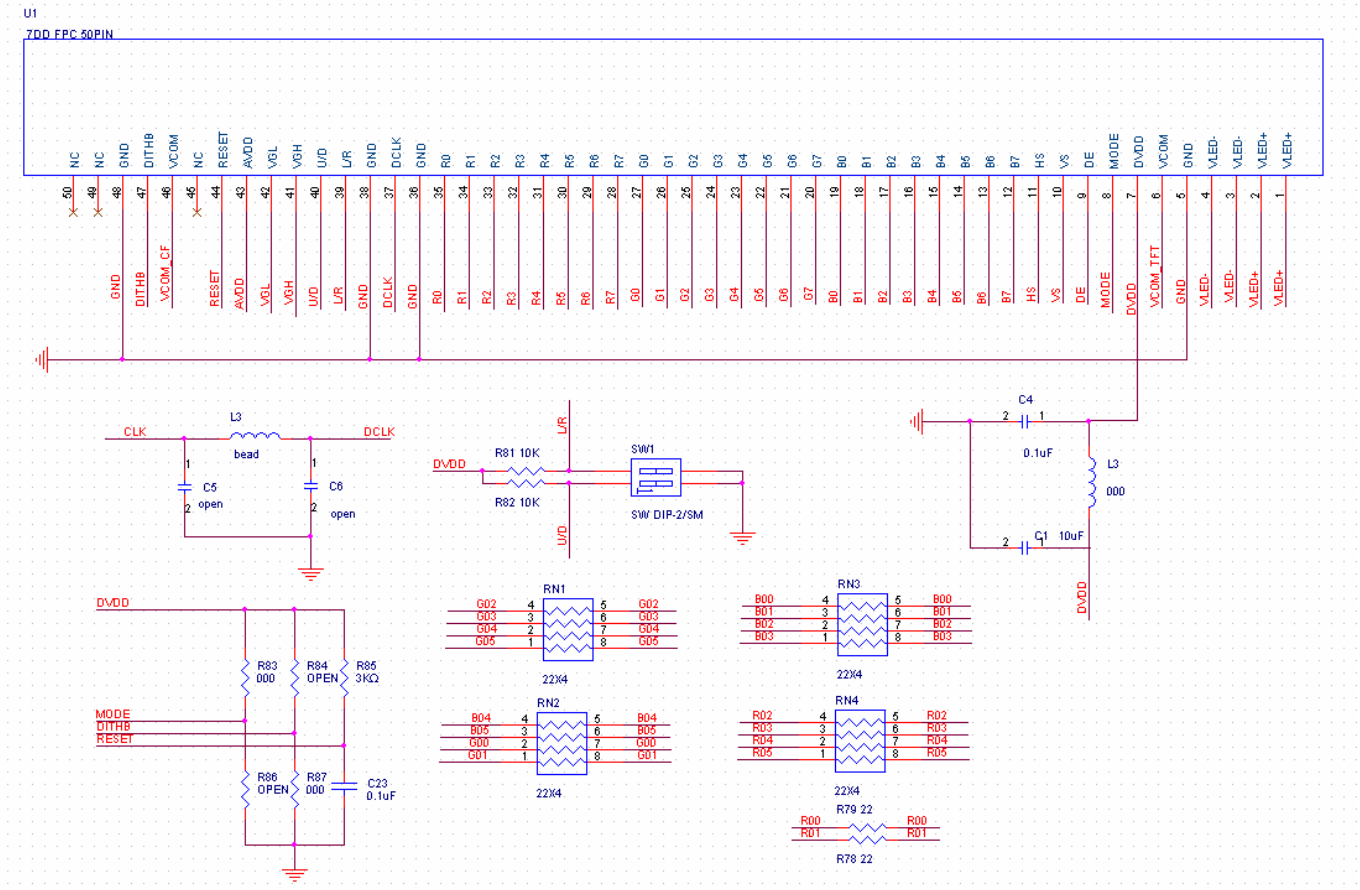
Figure 3. 2 Vertical input timing diagram.

4. Software Introduction

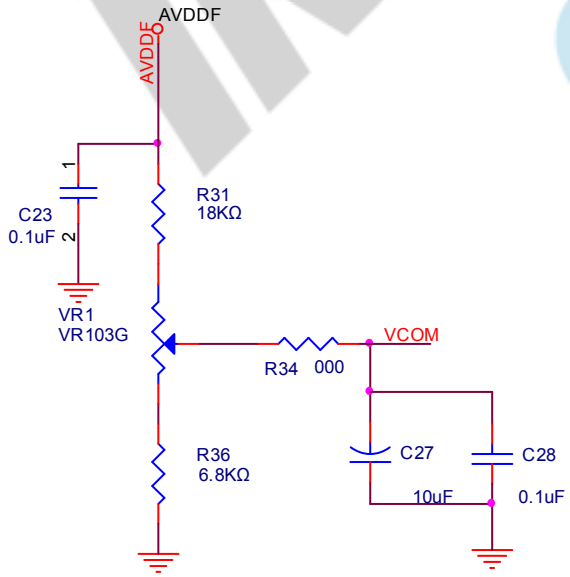
NA

5. Reference Circuit

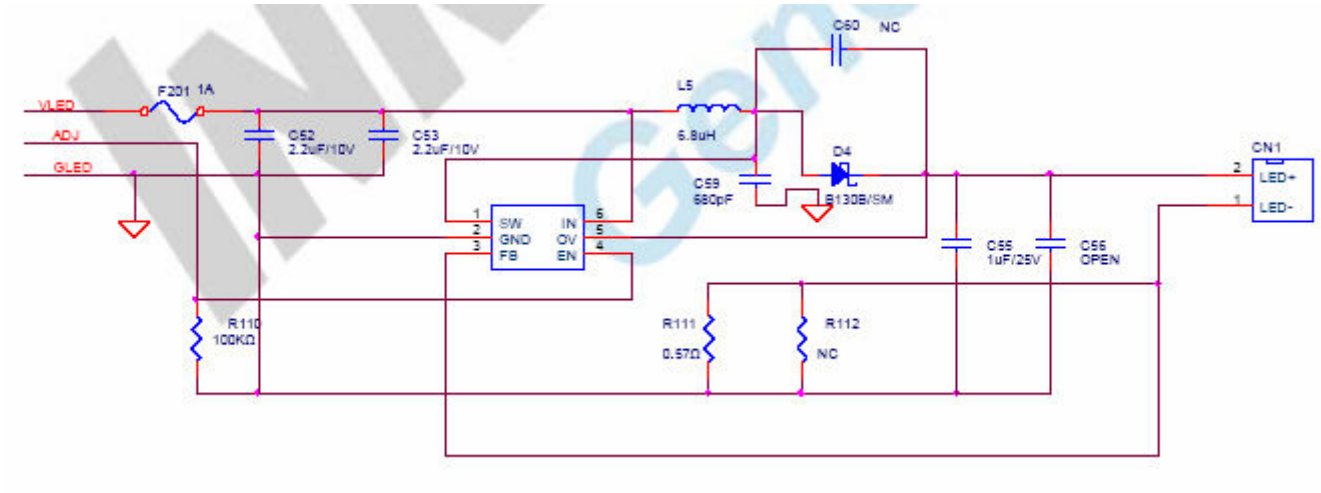
5.1 Interface reference circuit



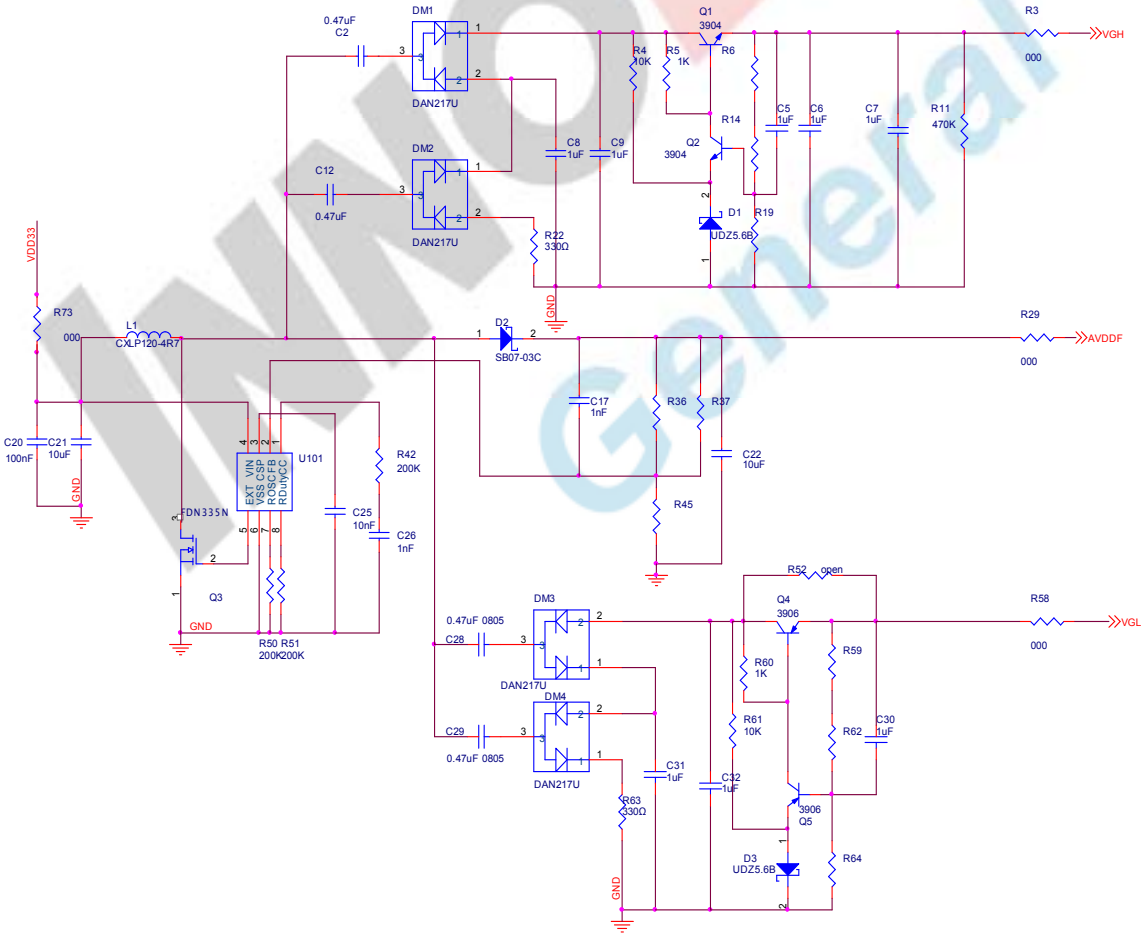
5.2 Vcom Reference Circuit



5.3 Backlight Driver Reference Circuit



5.4 DC/DC Reference Circuit



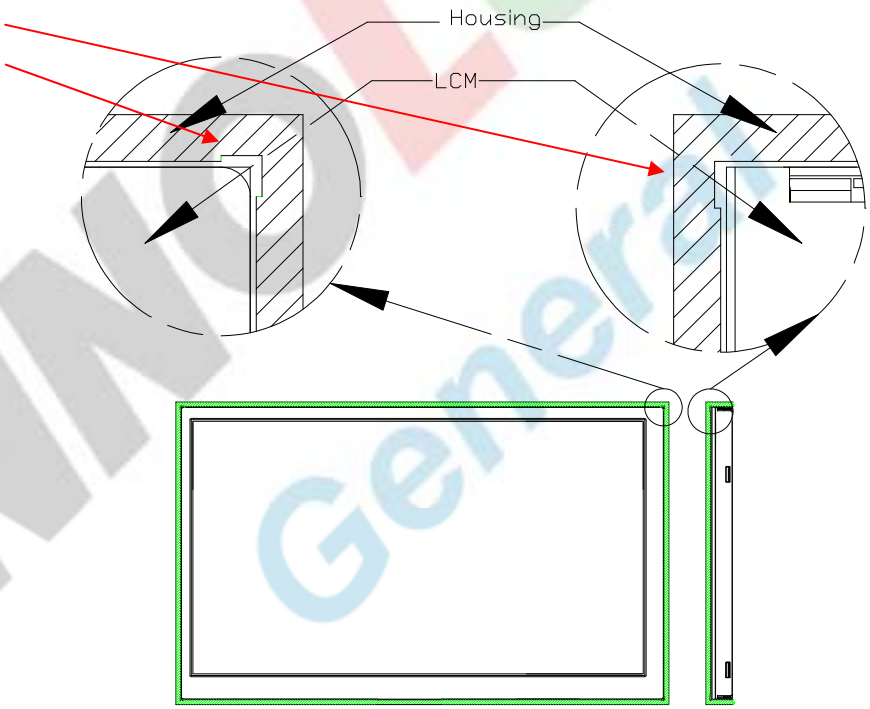
5.5 Vendor Recommend

Item	Vendor	Type	Remark
DC/DC	Fiti Power	FP6791	
LED Driver	Fiti Power	FP6745	PWM Frequency:100Hz~50KHz
	MPS	MPS3302	PWM Frequency:100Hz~20KHz

6.Suggestions for housing design.

6.1 LCM corner /edge avoidable cutting.

If you design a avoidable cutting as the right drawing. LCM will easier to assemble in the housing.
When you use the LCM with TSP, the cutting will avoid damage the edge or corner of TSP during the assembly.



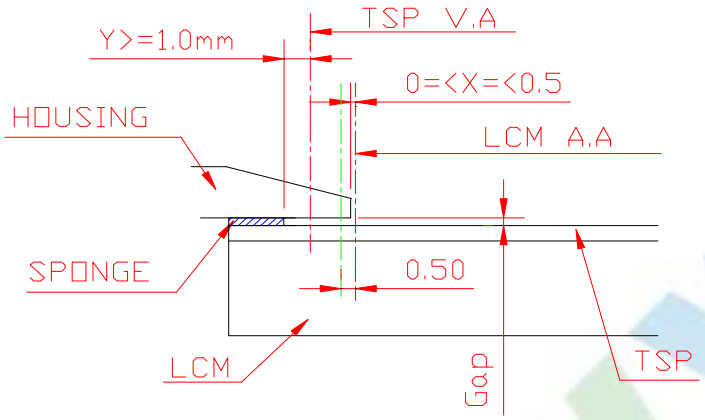
Suggestions of housing design

6.2 Housing opening design guide.

6.2.1 With TSP

Because touch film is made of flexible PET, any unexpected touch with it would cause malfunction of touch panel. So here a sponge between touch panel and plastic housing is

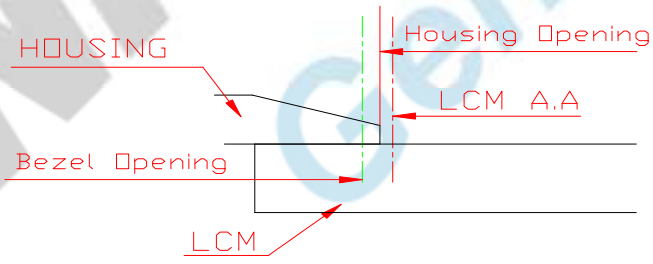
recommended for users. And the drawing will show you how to design the housing and sponge.



Section sketch (with TSP)

Notes: 1. X is the distance from LCM A.A to housing opening.
2. Y is the distance from TSP V.A to Sponge opening.
3. The active force will be bigger when you touch the area near the housing opening.
4. If you want to provide more protection for LCM, you can add same buffer material on the bottom of LCM.

6.2.2 Without TSP



Section sketch(without TSP)

Notes: 1. Housing opening mast bigger than LCMA.A and cover the bezel .
2. If you want to provide more protection for LCM, you can add same buffer material on the top or bottom of LCM.