CHIMEI INNOLUX DISPLAY CORPORATION

LCD MODULE

APPLICATION NOTE

Customer: 宇华微科技
LCD SIZE: 3.5”D
Date: 2010.07.28
Version: A

Remark
■ Single Power

Approved by	Reviewed by	Prepared by
Hans Chen 2010/07/28	David Tang 2010/07/28	Chunyan Huang 2010/07/28

Chimei Innolux Display Corporation
Industry District 10, LongHua, Shen, Ch
T.L +86-0755-27706888

Record of Revision

Version	Revise Date	Page	Content
A	2010/07/28		Initial Release

1. Module Introduction

1.1 Module Photo

Module Name	Module Photo	
	Top Side	Bottom Side
LQ035NC111		

1.2 Module Comparison Table

Module Name	Brightness(nits)	Pin Num.	Recommended Connector
LQ035NC111	300	54 Pins	FH28-54S-0.5SH(05)

2. Pin Assignment Table

Pin No.	Symbol	Function	Remark
1	LED-	Backlight LED Ground	
2	LED-	Backlight LED Ground	
3	LED+	Backlight LED Power	
4	LED+	Backlight LED Power	
5	NC	Not Use	
6	NC	Not Use	

7	NC	Not Use	
8	/RESET	Hardware Reset	
9	SPENA	SPI Interface Data Enable Signal	Note3
10	SPCLK	SPI Interface Data Clock	Note3
11	SPDAT	SPI Interface Data	Note3
12	B0	Blue Data Bit 0	
13	B1	Blue Data Bit 1	
14	B2	Blue Data Bit 2	
15	B3	Blue Data Bit 3	
16	B4	Blue Data Bit 4	
17	B5	Blue Data Bit 5	
18	B6	Blue Data Bit 6	
19	B7	Blue Data Bit 7	
20	G0	Green Data Bit 0	
21	G1	Green Data Bit 1	
22	G2	Green Data Bit 2	
23	G3	Green Data Bit 3	
24	G4	Green Data Bit 4	
25	G5	Green Data Bit 5	
26	G6	Green Data Bit 6	
27	G7	Green Data Bit 7	
28	R0	Red Data Bit0 /DX0	Note4
29	R1	Red Data Bit1 /DX1	Note4
30	R2	Red Data Bit2 /DX2	Note4
31	R3	Red Data Bit3 /DX3	Note4
32	R4	Red Data Bit4 /DX4	Note4
33	R5	Red Data Bit5 /DX5	Note4

34	R6	Red Data Bit6/DX6	Note4
35	R7	Red Data Bit7 /DX7	Note4
36	HSYNC	Horizontal Sync Input	
37	VSYNC	Vertical Sync Input	
38	DCLK	Dot Data Clock	
39	NC	Not Use	
40	NC	Not Use	
41	VCC	Digital Power	
42	VCC	Digital Power	
43	NC	Not Use	
44	NC	Not Use	
45	NC	Internal test use	
46	NC	Not Use	
47	NC	Internal test use	
48	SEL2	Control the input data format /floating	Note1
49	SEL1	Control the input data format	Note1
50	SEL0	Control the input data format	Note1
51	NC	Not Use	
52	DE	Data Enable Input	Note2
53	DGND	Ground	
54	AVSS		

Note:

1. The mode control (SEL2) not use, it can't control CCIR601 interface. If not use CCIR601, it can floating
2. For digital RGB input data format, both SYNC mode and DE+SYNC mode are supported. If DE signal is fixed now, SYNC mode is used. Otherwise, DE+SYNC mode is used. Suggest used SYNC mode. Suggest the DE signal usually pull low.
3. Usually pull high.
4. IF select serial RGB or CCIR601/656 input mode is selected, only DX0-DX7 used, and the other short to

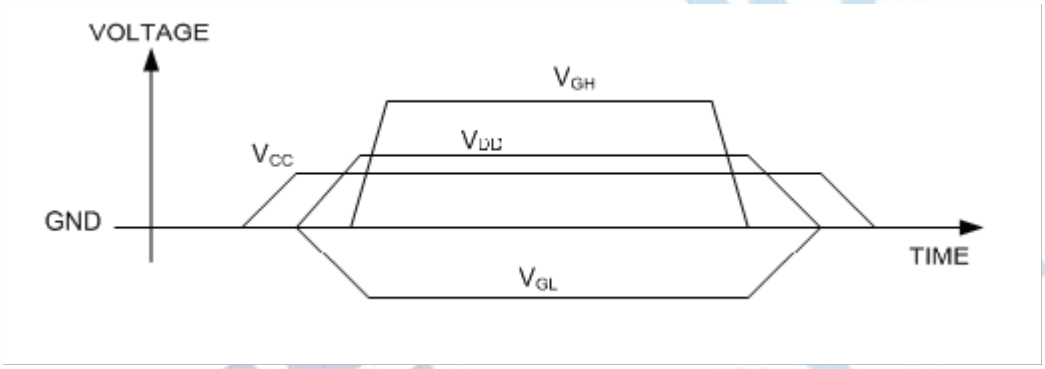
GND, only selected serial RGB、CCIR601/656 interface, DX BUS will enable. Digital input mode DX0 is LSB and DX7 is MSB.

3. Power &Timing Characteristic

3.1. Power Sequence

Customer should follow our product power sequence, other it would lead to display abnormal, please refer to the figures as below.

Power On:



Remark : Customer should follow every time, otherwise it maybe lead to display abnormal, you can refer our reference circuit.

3.2 Power Operation Conditions

Customer should notice the red mark specially, if you do not follow it, it would lead to display abnormal.

Parameter	Symbol	Rating			Unit	Condition
		Min.	Typ.	Max.		
Power Voltage	VCC	3.0	3.3	3.6	V	
Digital Operation Current	Icc	-	8.6	-	mA	
Gate On Power	VGH	-	13.9	-	V	
Gate Off Power	VGL	-	-13.6	-	V	
Vcom High Voltage	VcomH	-	3.9	-	V	Note1
Vcom low Voltage	VcomL	-	-1.2	-	V	Note1
Vcom level max	VcomA	-	-	6	V	

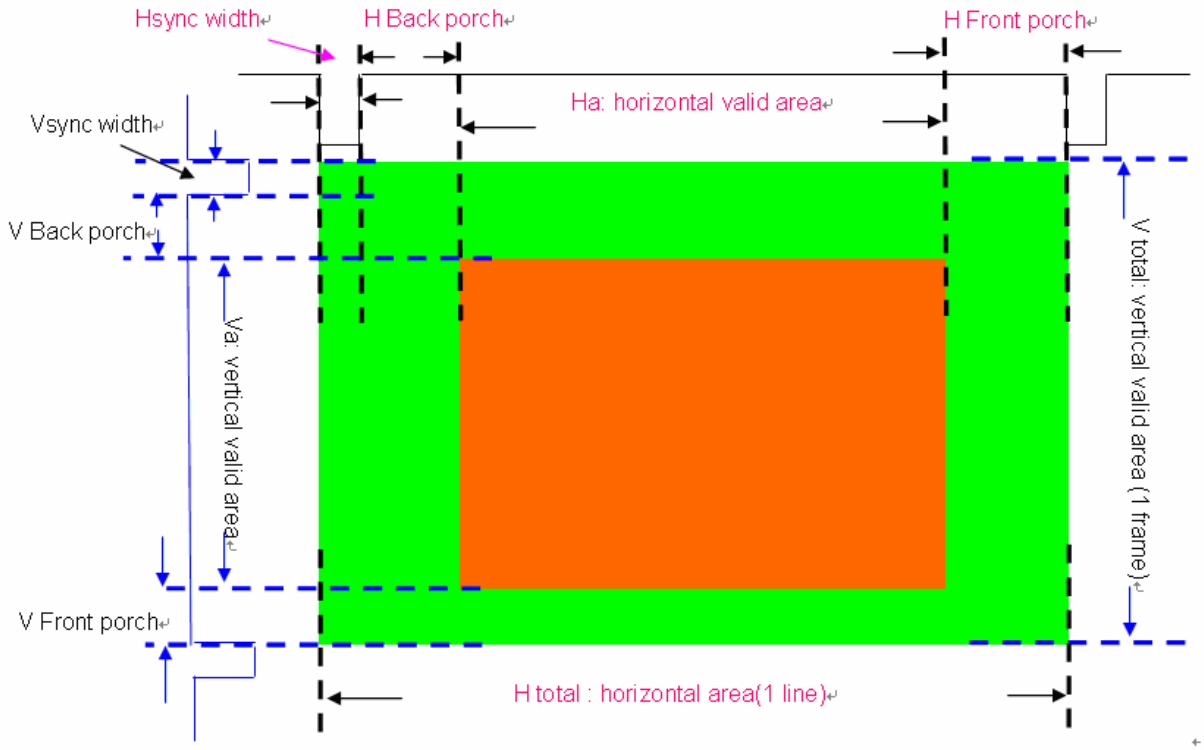
Note1. VcomH& VcomL：Adjust the color with gamma data. Vp-p should be higher then 4V.(Option 5V)

Parameter	Symbol	Rating			Unit	Condition
		Min.	Typ.	Max.		
Low level input voltage	V_{IL}	0	-	0.3 VCC	V	
Hight level input voltage	V_{IH}	0.7 VCC	-	VCC	V	

3.3 Timing Description

Our LCM has integrated T-con IC into our driver IC, so customer only input DCLK, HS, VS, DE and R/G/B data signals to our LCM from their system solution. But these signals must follow our timing specification. Otherwise the LCM will display abnormally.

We provide the Timing Drawing and Timing Formula for customer to how to set their parameters of LCD controller. About the detail timing parameters of LCD display, please follow the product specification.



Timing Drawing

Timing Formula:

DCLK = (Hw + Hbp + Ha +Hfp)*(Vw + Vbp + Va +Vfp)*Fvsync (Unit : Hz)

Fhsync = (Vw+ Vbp + Va +Vfp)*Fvsync (Unit : Hz)

Remark:

1. Fhsync is Hsync frequency, and Fvsync is Vsync frequency.

2. Parameter Table .

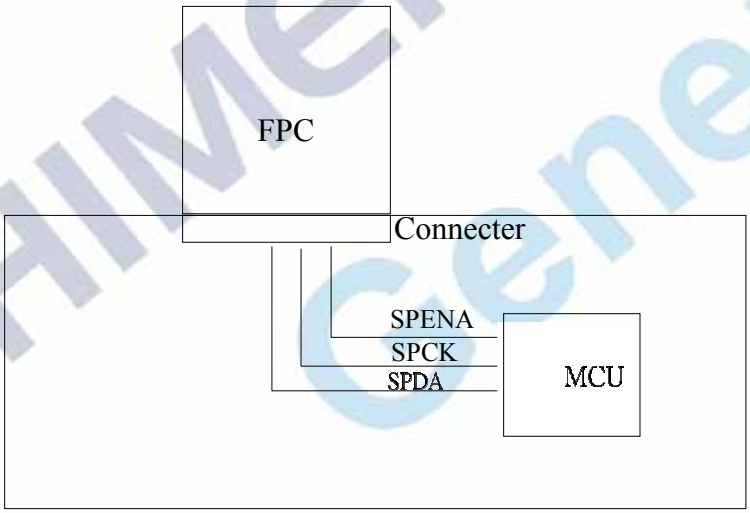
Parameter	Description	Unit
Hw	Hsync Width	DCLK
Hbp	Horizontal back porch	DCLK
Ha	Horizontal valid area	DCLK

Hfp	Horizontal front porch	DCLK
Vw	Vsync Width	Hsync(Line)
Vbp	Vertical back porch	Hsync(Line)
Va	Vertical valid area	Hsync(Line)
Vfp	Vertical front porch	Hsync(Line)
DCLK	Dot clock	Hz

4. Software Introduce

4.1 SPI Timing Characteristics

We suggest our customer refer to the below drawing to design SPI circuit. There are some special registers in the driver IC of 3.5” QVGA product. We must use Pin SPENA, SPCK, SPDA to set these registers. Only if set the correct value in these registers that the product will be displayed normally. Please refer to the product specification to set these values.



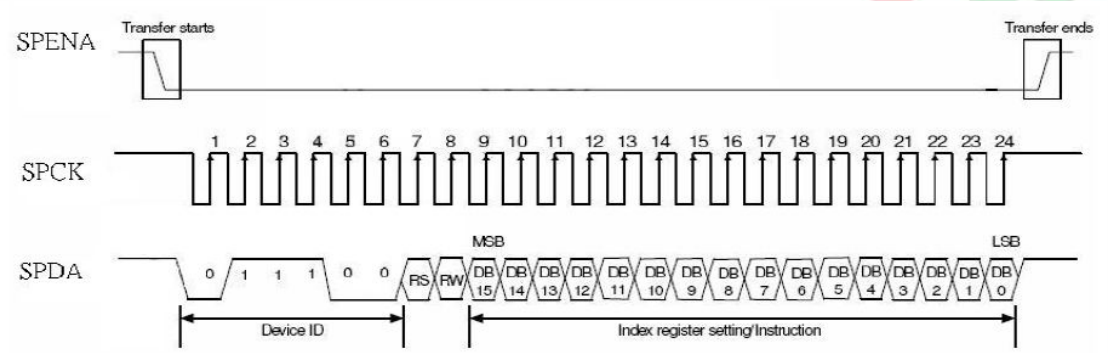
Customer system

3.5” QVGA products using the 3-wire serial port as communication interface for all the function and parameter setting. 3-wire communication can be bi-directional controlled by the “R/W” bit in address field. These products 3-Wire engine act as a “slave mode” for all the time, and will not issue any command to the 3-wire bus itself.

Under read mode, 3-Wire engine will return the data during “Data phase”. The returned data should be latched at the rising edge of SPCK by external controller. Data in the “Hi-Z phase” will be ignored by 3-Wire engine during write operation, and should be ignored during read operation

also. During read operation, external controller should float SPDA pin under “Hi-Z phase” and “Data phase”.

Each Read/Write operation should be exactly 16bit. To prevent form incorrect setting of the internal register any write operation with more of less the 16 bit data during a SPENB Low period will be ignored by 3-Wire engine.



4.2 Register Setting Table

Reg#	Hex Code	Register Bit Value
R01h	XX00	RL = X REV = X PINV = X BGR = X SM = “0” TB = X CPE = X
R02h	0200	B/C = “1”
R03h	6364	DCT = “0110” BT = “011” BTF = “0” DC = “0110” AP = “010”
R04h	04XX	PALM = “1” BLT = ”00” OEA = **note 2** SEL = X SWD = X
R05h		GHN=”1” XDK=”0” GDIS=”1” LPF=”1” DEP=”0” CKP=”1” VSP= **note 2** HSP=”0” DEO=”1” DIT=”1” PWM=”0” FB=”100”
R0Ah	4008	BR = “1000000” CON = “01000”
R0Bh	D400	NO = “11” SDT = “01” EQ = “100”
R0Dh	3229	VRC = “011” VDS = “10” VRH = “101001”
R0Eh	3200	VDV = “1001000”
R0Fh	0000	SCN = “00000000”
R16h	9F80	XLIM = “100111111”
R17h		STH = “00” HBP = **note 2** VBP = **note 2**
R1Eh	0052	nOTP = “0” VCM = “1010010”
R30h	0000	PKP1 = “000” PKP0 = “000”
R31h	0407	PKP3 = “100” PKP2 = “111”
R32h	0202	PKP5 = “010” PKP4 = “010”
R33h	0000	PRP1 = “000” PRP0 = “000”
R34h	0505	PKN1 = “101” PKN0 = “101”
R35h	0003	PKN3 = “000” PKN2 = “011”
R36h	0707	PKN5 = “111” PKN4 = “111”
R37h	0000	PRN1 = “000” PRN0 = “000”
R3Ah	0904	VRP1 = “01001” VRP0 = “0100”
R3Bh	0904	VRN1 = “01001” VRN0 = “0100”

Note: (1) X means the bit is refer to the logic stage of the corresponding hardware pin.
(2) The default values of the VSP、OEA、HBP、VBP are automatically set by SEL.

4.3 Register Function Description

4.3.1 Register Bit Definition

Reg#	Register	R/W	R/S	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
SR	Status Read	1	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0
R01h	Driver output control	0	1	0	RL	REV	PINV	BGR	SM	TB	CPE	0	0	0	0	0	0	0	0
R02h	LCD driver AC control	0	1	0	0	0	0	0	0	B/C	0	0	0	0	0	0	0	0	0
R03h	Power control (1)	0	1	DCT3	DCT2	DCT1	DCT0	BTF	BT2	BT1	BT0	DC3	DC2	DC1	DC0	AP2	AP1	AP0	0
R04h	Data and color filter control	0	1	0	0	0	0	0	PALM	BLT1	BLT0	OEA1	OEA0	SEL2	SEL1	SEL0	SWD2	SWD1	SWD0
R05h	Function control	0	1	GHN	XDK	GDIS	LPF	DEP	CKP	VSP	HSP	DEO	DIT	0	PWM	0	FB2	FB1	FB0
R06h	Reserved	Reserved																	
R07h	Reserved	Reserved																	
R0Ah	Contrast/ Brightness control	0	1	0	BR6	BR5	BR4	BR3	BR2	BR1	BR0	0	0	0	CON4	CON3	CON2	CON1	CON0
R0Bh	Frame cycle control	0	1	NO1	NO0	SDT1	SDT0	0	EQ2	EQ1	EQ0	0	0	0	0	0	0	0	0
R0Dh	Power control (2)	0	1	0	VRC2	VRC1	VRC0	0	0	VDS1	VDS0	0	0	VRH5	VRH4	VRH3	VRH2	VRH1	VRH0
R0Eh	Power control (3)	0	1	0	0	1	VDV6	VDV5	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0
R0Fh	Gate scan starting Position	0	1	0	0	0	0	0	0	0	0	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
R16h	Horizontal Porch	0	1	XLIM8	XLIM7	XLIM6	XLIM5	XLIM4	XLIM3	XLIM2	XLIM1	XLIM0	0	0	0	0	0	0	0
R17h	Vertical Porch	0	1	STH1	STH0	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0
R1Eh	Power control (4)	0	1	0	0	0	0	0	0	0	0	nOTP	VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
R27h	Reserved	Reserved																	
R28h	Reserved	Reserved																	
R29h	Reserved	Reserved																	
R2Bh	Reserved	Reserved																	
R30h	γ control (1)	0	1	0	0	0	0	0	PKP 12	PKP 11	PKP 10	0	0	0	0	0	PKP 02	PKP 01	PKP 00
R31h	γ control (2)	0	1	0	0	0	0	0	PKP 32	PKP 31	PKP 30	0	0	0	0	0	PKP 22	PKP 21	PKP 20
R32h	γ control (3)	0	1	0	0	0	0	0	PKP 52	PKP 51	PKP 50	0	0	0	0	0	PKP 42	PKP 41	PKP 40
R33h	γ control (4)	0	1	0	0	0	0	0	PRP 12	PRP 11	PRP 10	0	0	0	0	0	PRP 02	PRP 01	PRP 00
R34h	γ control (5)	0	1	0	0	0	0	0	PKN 12	PKN 11	PKN 10	0	0	0	0	0	PKN 02	PKN 01	PKN 00
R35h	γ control (6)	0	1	0	0	0	0	0	PKN 32	PKN 31	PKN 30	0	0	0	0	0	PKN 22	PKN 21	PKN 20
R36h	γ control (7)	0	1	0	0	0	0	0	PKN 52	PKN 51	PKN 50	0	0	0	0	0	PKN 42	PKN 41	PKN 40
R37h	γ control (8)	0	1	0	0	0	0	0	PRN 12	PRN 11	PRN 10	0	0	0	0	0	PRN 02	PRN 01	PRN 00
R3Ah	γ control (9)	0	1	0	0	0	VRP 14	VRP 13	VRP 12	VRP 11	VRP 10	0	0	0	0	VRP 03	VRP 02	VRP 01	VRP 00
R3Bh	γ control (10)	0	1	0	0	0	VRN 14	VRN 13	VRN 12	VRN 11	VRN 10	0	0	0	0	VRN 03	VRN 02	VRN 01	VRN 00

Note: * means don't care
Software settings will override hardware pin (eg, BGR bits override BGR pin definition)

4.3.2 Register Function Description

Status Read

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0

Figure 9. 1 Status Read

The status read instruction reads the internal status of the HX8238-A.

L7–0: Indicate the driving raster-row position where the liquid crystal display is being driven.

Driver Output Control (R01h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	R_L	REV	PINV	BGR	S_M	T_B	CPE	0	0	0	0	0	0	0	0

Figure 9. 2 Driver Output Control

CPE: When CPE=0, Vcim is not shut down, but VGH, VGL, and Vcix2 are shut down. When CPE=1, internal charge pump Vcim, VGH, VGL, and Vcix2 are enabled.

REV: Displays all character and graphics display sections with reversal when REV = "0". Since the grayscale level can be reversed, display of the same data is enabled on normally white and normally black panels. Source output level is indicated below.

REV	RGB data	Source output level	
		VCOM = "L"	VCOM = "H"
1	00000H : 3FFFFH	V0 : V63	V63 : V0
0	00000H : 3FFFFH	V63 : V0	V0 : V63

Table 9. 1 Source Output Level

PINV: When PINV=0, POL output is same phase with internal VCOM signal. When PINV=1, POL output phase is reversed with VCOM signal.

BGR: Selects the <R><G><B> arrangement. When BGR = "0" <R><G><B> color is assigned from S0.When BGR = "1" <B><G><R> color is assigned from S0.

SM: Change the division of gate driver. When SM = "0", odd/even division (interlace mode) is selected. When SM = "1", upper/lower division is selected. Select the division mode according to the mounting method.

TB: Selects the output shift direction of the gate driver. When TB = "1", G0 shifts to G239. When TB = "0", G239 shifts to G0.

RL: Selects the output shift direction of the source driver. When RL = "1", S0 shifts to S959 and <R><G><B> color is assigned from S0. When RL = "0", S959 shifts to S0 and <R><G><B> color is assigned from S959. Set RL bit and BGR bit when changing the dot order of R, G and B.

Note: The default setting of register bits REV, BGR, TB and RL are defined by the logic stage of corresponding hardware pins. These bits will override the hardware setting once software command was sent to set the bits.

LCD-Driving-Waveform Control (R02h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	B/C	0	0	0	0	0	0	0	0	0

Figure 9. 4 LCD-Driving-Waveform Control

B/C: When B/C = 0, frame inversion of the LCD driving signal is enabled. When B/C = 1, line inversion waveform is generated

Power control 1 (R03h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	DCT3	DCT2	DCT1	DCT0	BTF	BT2	BT1	BT0	DC3	DC2	DC1	DC0	AP2	AP1	AP0	0

Figure 9. 5 Power Control 1

DCT3-0: Set the step-up cycle of the step-up circuit for 8-color mode (CM = VDDIO). When the cycle is accelerated, the Vcim and Vcix2 driving ability of the step-up circuit increase, but their current consumption increase, too. Adjust the cycle taking into account the display quality and power consumption. VGH and VGL are always fixed at the step-up cycle of Fline x 0.5.

DCT3	DCT2	DCT1	DCT0	Step-up cycle
0	0	0	0	Fline x 14
0	0	0	1	Fline x 12
0	0	1	0	Fline x 10
0	0	1	1	Fline x 8
0	1	0	0	Fline x 7
0	1	0	1	Fline x 6
0	1	1	0	Fline x 5
0	1	1	1	Fline x 4
1	0	0	0	Fline x 3
1	0	0	1	Fline x 2
1	0	1	0	Fline x 1
1	0	1	1	Fline x 0.5
1	1	0	0	Fline x 0.25
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

* Fline – horizontal frequency (Fline Typ. 15KHz)

Table 9. 2 Step-up Cycle

BT2-0 & BTF: Control the step-up factor of the step-up circuit. Adjust the step-up factor according to the power supply voltage to be used.

BTF	BT2	BT1	BT0	VGH output	VGL output
0	0	0	0	VCIx2j X 3	- (VCIx2j X 3) + VCI
0	0	0	1	VCIx2j X 3	- (VCIx2j X 2)
0	0	1	0	VCIx2 j X 3	- (VCIx2j X 3)
0	0	1	1	VCIx2j X 2 + VCI	- (VCIx2j X 2) - VCI
0	1	0	0	VCIx2j X 2 + VCI	- (VCIx2j X 2)
0	1	0	1	VCIx2j X 2 + VCI	- (VCIx2j X 2) + VCI
0	1	1	0	VCIx2j X 2	- (VCIx2j X 2)
0	1	1	1	VCIx2j X 2	- (VCIx2j X 2) + VCI
1	X	X	X	VCIx2j X 3	- VCIx2j

Table 9. 3 VGH and VGL Booster Ratio

DC3-0: Set the step-up cycle of the step-up circuit for 262k-color mode (CM = VSS). When the cycle is accelerated, the Vcim and Vcix2 driving ability of the step-up circuit increase, but their current consumption increase, too. Adjust the cycle taking into account the display quality and power consumption.
VGH and VGL are always fixed at the step-up cycle of Fline x 0.5.

DC3	DC2	DC1	DC0	Step-up cycle
0	0	0	0	Fline x 14
0	0	0	1	Fline x 12
0	0	1	0	Fline x 10
0	0	1	1	Fline x 8
0	1	0	0	Fline x 7
0	1	0	1	Fline x 6
0	1	1	0	Fline x 5
0	1	1	1	Fline x 4
1	0	0	0	Fline x 3
1	0	0	1	Fline x 2
1	0	1	0	Fline x 1
1	0	1	1	Fline x 0.5
1	1	0	0	Fline x 0.25
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

Note: Fline = horizontal frequency (Fline Typ. 15KHz)

Table 9. 4 Step-up Cycle

AP2-0: Adjust the amount of current from the stable-current source in the internal operational amplifier circuit. When the amount of current becomes large, the driving ability of the operational-amplifier circuits increase. Adjust the current taking into account the power consumption. During times when there is no display, such as when the system is in a sleep mode, set AP2-0 = "000" to halt the operational amplifier circuit and the step-up circuits to reduce current consumption.

AP2	AP1	AP0	Op-amp power
0	0	0	Least
0	0	1	Small
0	1	0	Small to medium
0	1	1	Medium
1	0	0	Medium to large
1	0	1	Large
1	1	0	Large to Maximum
1	1	1	Maximum

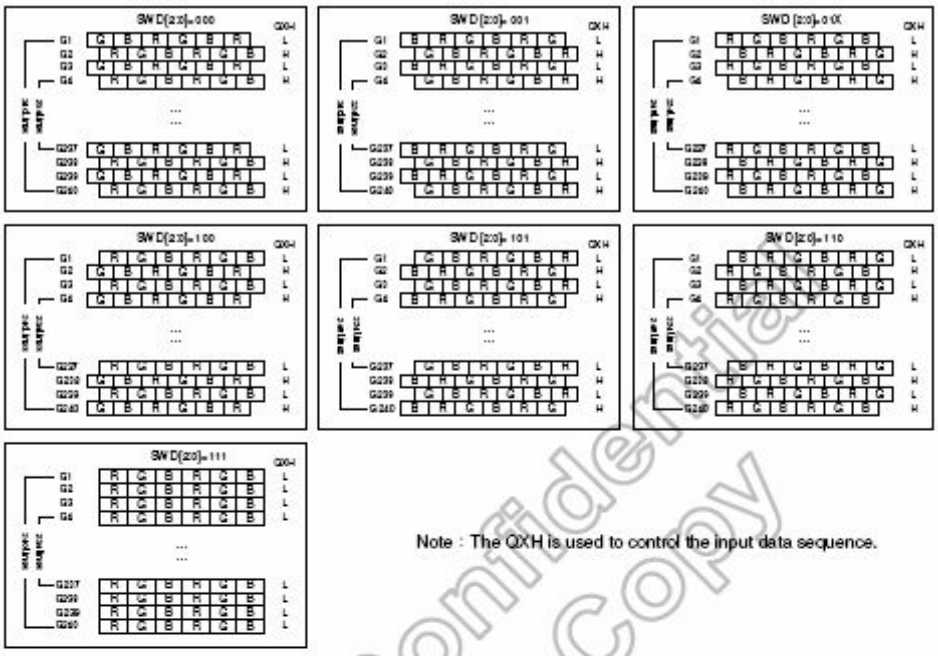
Table 9. 5 Op-amp Power

Input Data and Color Filter Control (R04h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PALN	BLT1	BLT0	OGA1	OGA0	SEL2	SEL1	SEL0	SWD2	SWD1	SWD0

Figure 9. 6 Input Data and Color Filter Control

SWD2-0: Control and switch the relationship between the R, G, B data and color filter type.



Note : The QXH is used to control the input data sequence.

Table 9. 6 Color Filter Type

SEL2-0: Define the input interface mode.

SEL2	SEL1	SEL0	Format	Operating Frequency
0	0	0	Parallel-RGB data format (only support stripe type color filter)	6.5MHz
0	0	1	Serial-RGB data format	19.5MHz
0	1	0	CCIR 656 data format (640RGB)	24.54MHz
0	1	1	CCIR 656 data format (720RGB)	27MHz
1	0	0	YUV mode A data format (Cr-Y-Cb-Y)	24.54MHz
1	0	1	YUV mode A data format (Cr-Y-Cb-Y)	27MHz
1	1	0	YUV mode B data format (Cb-Y-Cr-Y)	27MHz
1	1	1	YUV mode B data format (Cb-Y-Cr-Y)	24.54MHz

Input format	DOTCLK Freq (MHz)	Display Data	Active Area (DOTCLK)
YUV mode	24.54	640	1280
	27	720	1440

Table 9. 7 Interface Type

OEA1-0: Odd/Even field advanced function.

OEA1	OEA0	
0	0	Display Start @ VBP delay for Odd field and @ ***VBP-1*** for Even field.
0	1	Display Start @ VBP delay for Odd field and @ ***VBP*** for Even field.
1	0	Display Start @ VBP delay for Odd field and @ ***VBP+1*** for Even field.
1	1	No use

Table 9. 8 Odd/Even Field Advanced Function

BLT [1:0]: Set the initial power on black image insertion time.
00: 10 fields
01: 20 fields
10: 40 fields
11: 80 fields

PALM: Set the input data line number in PAL mode
0: 280 lines
1: 288 lines

Function Control (R05h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	GHN	XDK	GDIS	LPF	DEP	CKP	VSP	HSP	DEO	DIT	0	PWM	0	FB2	FB1	FB0

Figure 9. 7 Function control

FB2-0: Set PWM feedback level adjustment.
000: 0.4V
001: 0.45V
010: 0.5V
011: 0.55V
100: 0.6V
101: 0.65V
110: 0.7V
111: 0.75V

PWM: When PWM=0, PWM function is disabled. When PWM=1, PWM function is enabled.

DIT: When DIT=0, dithering function is turned off. When DIT=1, dithering function is enabled.

DEO: When DEO=0, VSYNC/HSYNC are also needed in DE mode. Under this condition, vertical back porch is defined by VBP [6:0] and the horizontal first valid data is defined by DE signal. When DEO=1, only DEN signal is needed in DE mode.

HSP: When HSP=0, HSYNC is negative polarity. When HSP=1, HSYNC is positive polarity.

VSP: When VSP=0, VSYNC is negative polarity. When VSP=1, VSYNC is positive polarity.

CKP: When CKP=0, data is latched in CLK falling edge. When CKP=1, data is latched by CLK rising edge.

DEP: When DEP=0, DEN is negative polarity active. When DEP=1, DEN is positive polarity active.

LPF: When LPF=0, the low pass filter function in YUV mode is disabled. When LPF=1, the low pass filter function is YUV mode is enabled.

GDIS: When GDIS=0, VGL has no discharge path to VSS in standby mode. When GDIS=1, VGL will discharge to VSS in standby mode. When CPE=0, GDIS is fixed to 0, and you can't change it by SPI.

XDK: When XDK=0, VCIX2 is 2 stage pumping from VCI. (VCIX2=3 x VCI) When XDK=1, VCIX2 is 2 phase pumping from VCI. (VCIX2=2 x VCI)

GHN: When GHN=0, all gate outputs are forced to VGH. When GHN=1, gate driver is normal operation.

Contrast/Brightness Control (R0Ah)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	BR6	BR5	BR4	BR3	BR2	BR1	BR0	0	0	0	CON4	CON3	CON2	CON1	CON0

Figure 9. 8 Contrast/Brightness Control

CON4-0: Display Contrast level adjustment. (0.125/step) Adjust range from 00h (level = 0) to 1Fh (level = 3.875). Default value is 08h (level = 1).
BR6-0: Display Brightness level adjustment. (2/step) Adjust range from 00h (level = -128) to 7Fh (level = +126). Default value is 40h (level = 0).

Frame Cycle Control (R0Bh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	NO1	NO0	SDT1	SDT0	0	EQ2	EQ1	EQ0	0	0	0	0	0	0	0	0

Figure 9. 9 Frame Cycle Control

NO1-0: Sets amount of non-overlap of the gate output.

NO1	NO0	Amount of non-overlap
0	0	1.5 us
0	1	3 us
1	0	4.5 us
1	1	6 us

Table 9. 9 Amount of Non-overlap

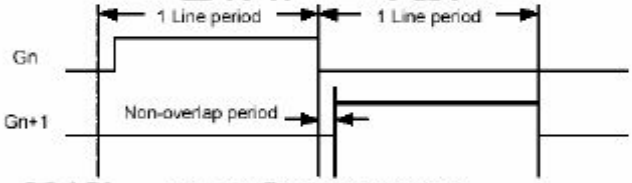


Figure 9. 10 NO Timing Diagram

SDT1-0: Set delay amount from the gate output signal falling edge to the source outputs.

SDT1	SDT0	Delay amount of the source output
0	0	1 us
0	1	3 us
1	0	5 us
1	1	7 us

Table 9. 10 Delay Amount of Source Output

EQ2-0: Sets the equalizing period.

EQ2	EQ1	EQ0	EQ period
0	0	0	No EQ
0	0	1	3 us
0	1	0	4 us
0	1	1	5 us
1	0	0	6 us
1	0	1	7 us
1	1	0	8 us
1	1	1	9 us

Table 9. 11 EQ Period

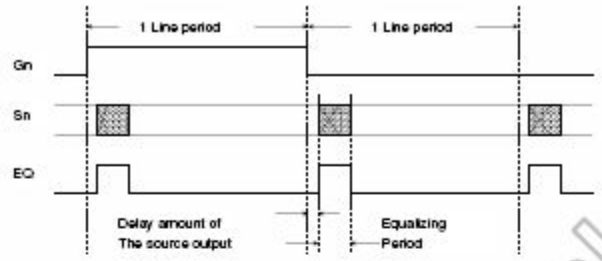


Figure 9. 11 EQ Timing Diagram

Power Control 2 (R0Dh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	VRC2	VRC1	VRC0	0	0	VDS1	VDS0	0	0	VRH5	VRH4	VRH3	VRH2	VRH1	VRH0

Figure 9. 12 Power Control 2

VRC [2:0]: set the VCIX2 charge pump voltage clamp.
VRC [2:0]=000, 5.1V
VRC [2:0]=001, 5.3V
VRC [2:0]=010, 5.5V
VRC [2:0]=011, 5.7V
VRC [2:0]=100, 5.9V
VRC [2:0]=101, reserved
VRC [2:0]=110, reserved
VRC [2:0]=111, reserved

VDS [1:0]: set the VDD regulator voltage if pin "REGVDD" is set to VDDIO.
VDS [1:0]=00, 1.8V
VDS [1:0]=01, 2.0V
VDS [1:0]=10, 2.2V
VDS [1:0]=11, 2.5V

VRH5-0: Set amplitude magnification of VLCD63. These bits amplify the VLCD63 voltage 2.464 to 4.456 times the Vref voltage set by VRH5-0.

Power Control 3 (R0Eh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	1	VDV6	VDV5	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0

Figure 9. 13 Power Control 3

VDV6-0: Set the alternating amplitudes of VCOM at the VCOM alternating drive. These bits amplify VCOM amplitude 0.6 to 1.2525 times the VLCD63 voltage. External voltage at VCOMR is referenced when VDV = "01111xx".

VDV6	VDV5	VDV4	VDV3	VDV2	VDV1	VDV0	VCOM Amplitude
0	0	0	0	0	0	0	VLCD63 x 0.6000
0	0	0	0	0	0	1	VLCD63 x 0.6075
0	0	0	0	0	1	0	VLCD63 x 0.6150
0	0	0	0	0	1	1	VLCD63 x 0.6225
0	0	0	0	1	0	0	VLCD63 x 0.6300
:	:	:	:	:	:	:	: Step = 0.0075 :
0	1	1	1	0	1	0	VLCD63 x 1.0350
0	1	1	1	0	1	1	VLCD63 x 1.0425
0	1	1	1	1	*	*	Reference from external voltage (VCOMR)
1	0	0	0	0	0	0	VLCD63 x 1.0500
1	0	0	0	0	0	1	VLCD63 x 1.0575
:	:	:	:	:	:	:	: Step = 0.0075 :
1	0	1	1	0	1	0	VLCD63 x 1.2450
1	0	1	1	0	1	1	VLCD63 x 1.2525
1	0	1	1	1	*	*	Reserved
1	1	*	*	*	*	*	Reserved

Table 9. 13 VCOM Amplitude

Gate Scan Position (R0Fh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0

Figure 9. 14 Gate Scan Position

SCN8-0: Set the scanning starting position of the gate driver.

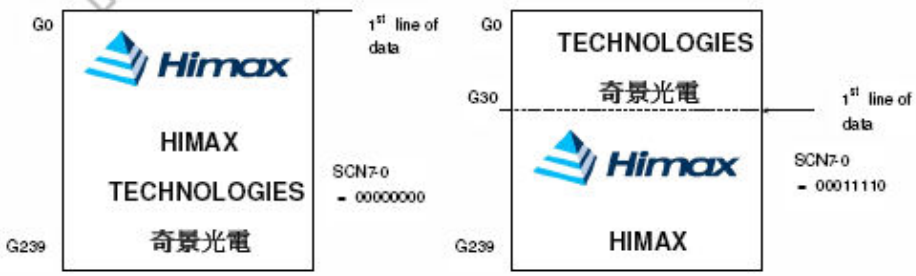


Figure 9. 15 Gate scan display position

Horizontal Porch (R16h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	XLIM8	XLIM7	XLIM6	XLIM5	XLIM4	XLIM3	XLIM2	XLIM1	XLIM0	0	0	0	0	0	0	0

Figure 9. 16 Horizontal Porch

XLIM8-0: Set the number of valid pixel per line.

XLIM8	XLIM7	XLIM6	XLIM5	XLIM4	XLIM3	XLIM2	XLIM1	XLIM0	No. of pixel per line
0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	0	1	0	3
:	:	:	:	:	:	:	:	:	: Step = 1 :
1	0	0	1	1	1	1	1	0	319
1	0	0	1	1	1	1	1	1	320
1	0	1	*	*	*	*	*	*	Reserved
1	1	*	*	*	*	*	*	*	Reserved

Table 9. 14 No. of Pixel Per Line

Vertical Porch (R17h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	STH1	STH0	HBP8	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	VBP8	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0

Figure 9. 17 Vertical Porch

HBP6-0: Set the delay period from falling edge of HSYNC signal to first valid data. The pixel data exceed the range set by XLIM8-0 and before the first valid data will be treated as dummy data. The setting is only effective in SYNC mode timing.

HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	No. of Clock Cycle
0	0	0	0	0	0	0	Can't set
0	0	0	0	0	0	1	Can't set
0	0	0	0	0	1	0	Can't set
0	0	0	0	0	1	1	Can't set
0	0	0	0	1	0	0	Can't set
0	0	0	0	1	0	1	Can't set
0	0	0	0	1	1	0	Can't set
0	0	0	0	1	1	1	Can't set
0	0	0	1	0	0	0	Can't set
0	0	0	1	0	0	1	9
							: Step = 1 :
1	1	1	1	1	1	0	126
1	1	1	1	1	1	1	127

Table 9. 15 No. of Clock Cycle of Clock

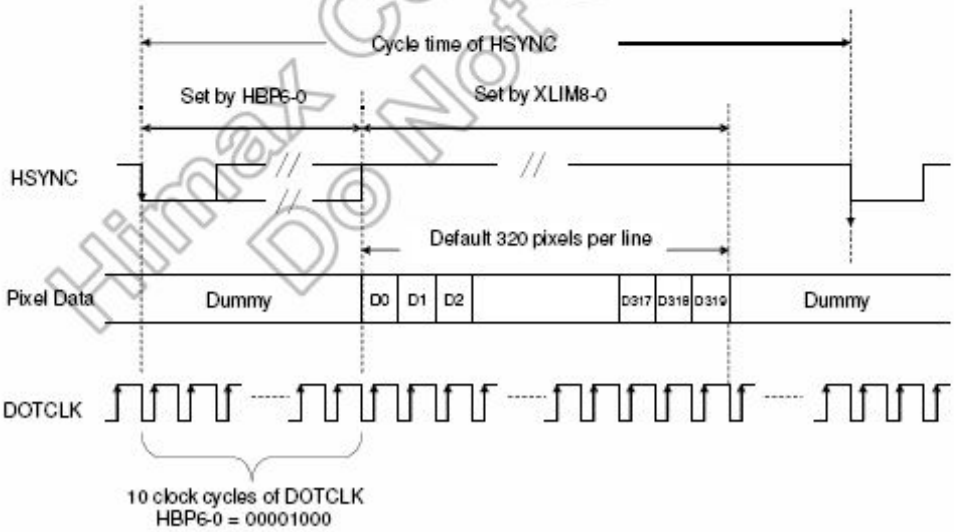


Figure 9. 18 No. of Clock Cycle of Clock

STH1-0: Adjust the first valid data by dot clock. This setting is not valid in parallel RGB input interface.
STH = 00: +0 dot clock
STH = 01: +1 dot clock
STH = 10: +2 dot clock
STH = 11: +3 dot clock

VBP6-0: Set the delay period from falling edge of VSYNC to first valid line. The line data within this delay period will be treated as dummy line. The setting is only effective in SYNC mode timing.

VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0	No. of clock cycle of HSYNC
0	0	0	0	0	0	0	Can't set
0	0	0	0	0	0	1	Can't set
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
0	0	0	0	1	0	0	4
							: Step = 1 :
1	1	1	1	1	0	0	124
1	1	1	1	1	0	1	125
1	1	1	1	1	1	0	126
1	1	1	1	1	1	1	127

Table 9. 16 No. of Clock Cycle of HSYNC

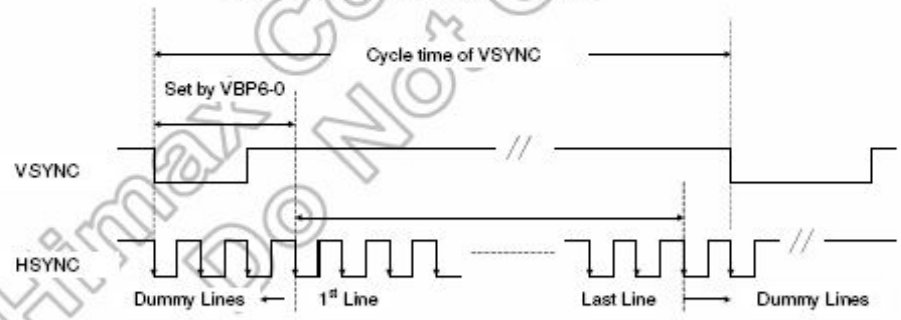


Figure 9. 19 No. of Clock Cycle of HSYNC

Power Control 4 (R1Eh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	nOTP	VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0

Figure 9. 20 Power Control 4

nOTP: nOTP equals to "0" after power on reset and VCOMH voltage equals to programmed OTP value. When nOTP set to "1", setting of VCM6-0 becomes valid and voltage of VCOMH can be adjusted.

VCM6-0: Set the VCOMH voltage if nOTP = "1". These bits amplify the VCOMH voltage 0.36 to 0.995 times the VLCD63 voltage.

VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	VCOMH
0	0	0	0	0	0	0	VLCD63 x 0.360
0	0	0	0	0	0	1	VLCD63 x 0.365
0	0	0	0	0	1	0	VLCD63 x 0.370
0	0	0	0	0	1	1	VLCD63 x 0.375
0	0	0	0	1	0	0	VLCD63 x 0.380
			:			:	:
							Step = 0.005
			:			:	:
1	1	1	1	1	0	0	VLCD63 x 0.980
1	1	1	1	1	0	1	VLCD63 x 0.985
1	1	1	1	1	1	0	VLCD63 x 0.990
1	1	1	1	1	1	1	VLCD63 x 0.995

Note: 2V < VCOMH < VLCD63

Table 9. 17 VCOMH

Gamma Control 1 (R30h to R37h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PKP1	PKP1	PKP1	0	0	0	0	0	PKP0	PKP0	PKP0
W	1	0	0	0	0	0	PKP3	PKP3	PKP3	0	0	0	0	0	PKP2	PKP2	PKP2
W	1	0	0	0	0	0	PKP5	PKP5	PKP5	0	0	0	0	0	PKP4	PKP4	PKP4
W	1	0	0	0	0	0	PRP1	PRP1	PRP1	0	0	0	0	0	PRP0	PRP0	PRP0
W	1	0	0	0	0	0	PKN1	PKN1	PKN1	0	0	0	0	0	PKN0	PKN0	PKN0
W	1	0	0	0	0	0	PKN3	PKN3	PKN3	0	0	0	0	0	PKN2	PKN2	PKN2
W	1	0	0	0	0	0	PKN5	PKN5	PKN5	0	0	0	0	0	PKN4	PKN4	PKN4
W	1	0	0	0	0	0	PRN1	PRN1	PRN1	0	0	0	0	0	PRN0	PRN0	PRN0

Figure 9. 21 Gamma Control 1

PKP52–00: Gamma micro adjustment registers for the positive polarity output.
PRP12-00: Gradient adjustment registers for the positive polarity output.
PKN52-00: Gamma micro adjustment registers for the negative polarity output.
PRN12-00: Gradient adjustment registers for the negative polarity output.

Gamma Control 2 (R3Ah to R3Bh)

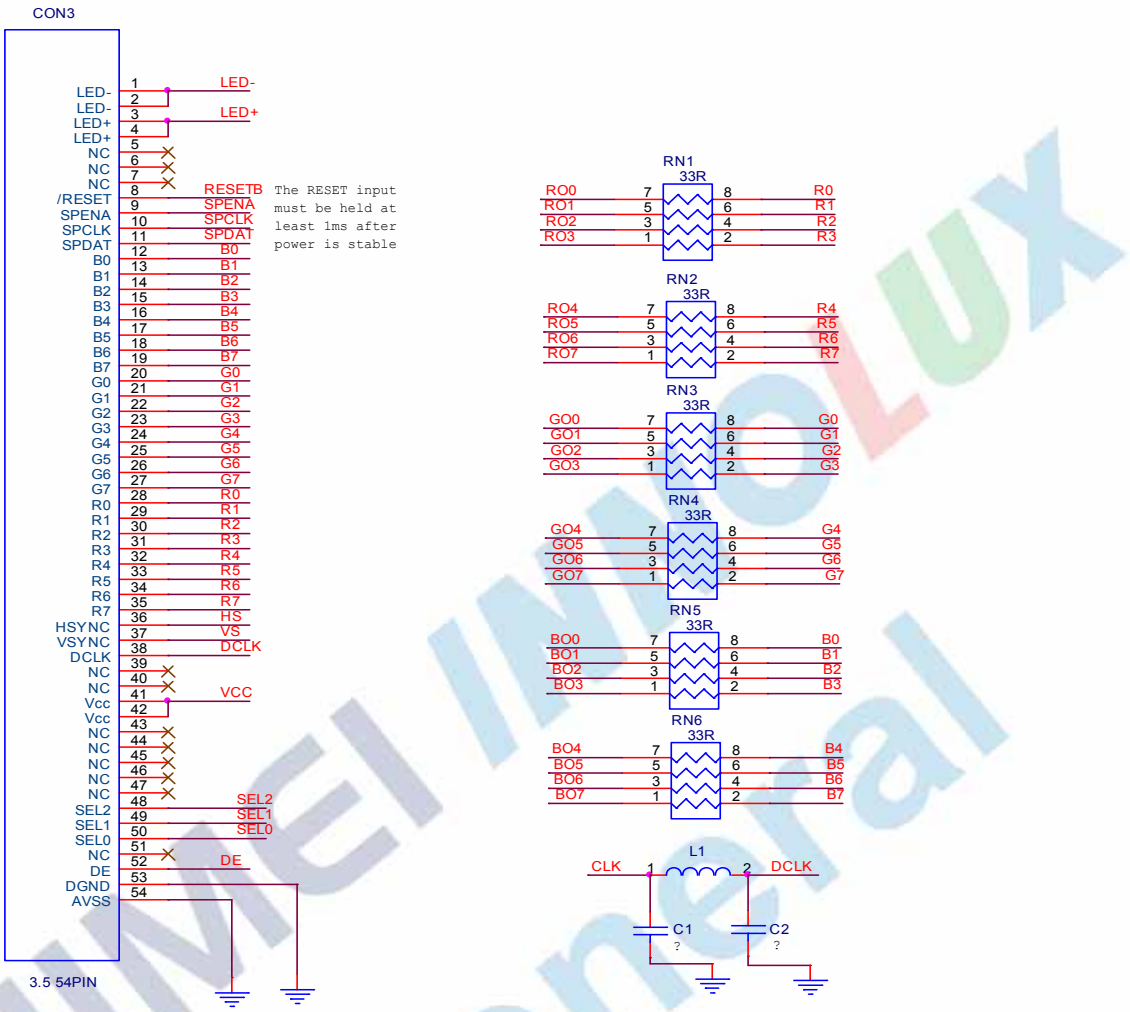
R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	VRP14	VRP13	VRP12	VRP11	VRP10	0	0	0	0	VRP03	VRP02	VRP01	VRP00
W	1	0	0	0	VRN14	VRN13	VRN12	VRN11	VRN10	0	0	0	0	VRN03	VRN02	VRN01	VRN00

Figure 9. 22 Gamma Control 2

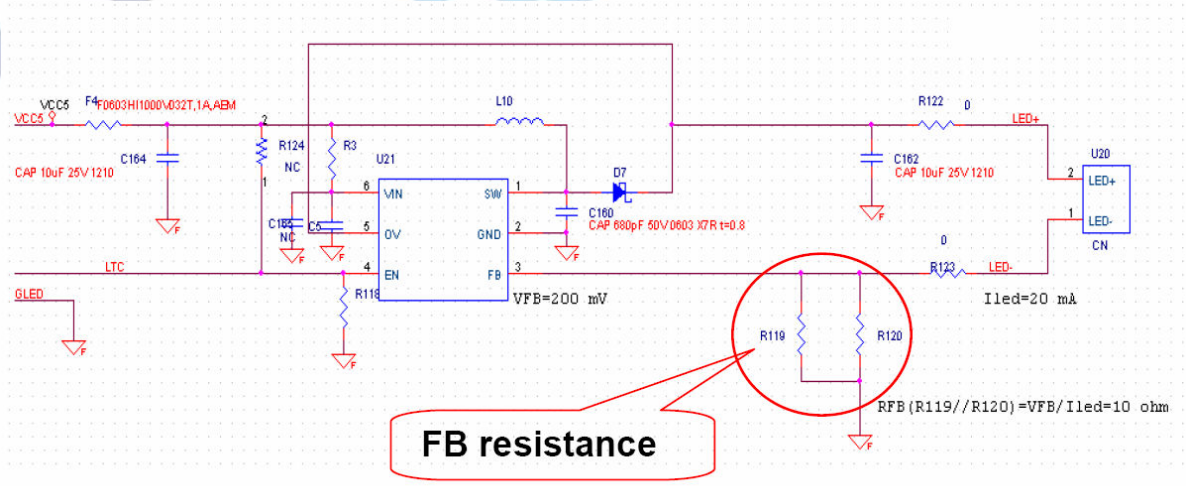
VRP14-00: Adjustment registers for amplification adjustment of the positive polarity output.
VRN14-00: Adjustment registers for the amplification adjustment of the negative polarity output.
(Refer to Gamma Adjustment Function for details)

5. Reference Circuit

5.1 Interface reference circuit



5.2 Backlight Driver Reference Circuit



Note：$I_{LED}=V_{FB}/(R119//R120)$

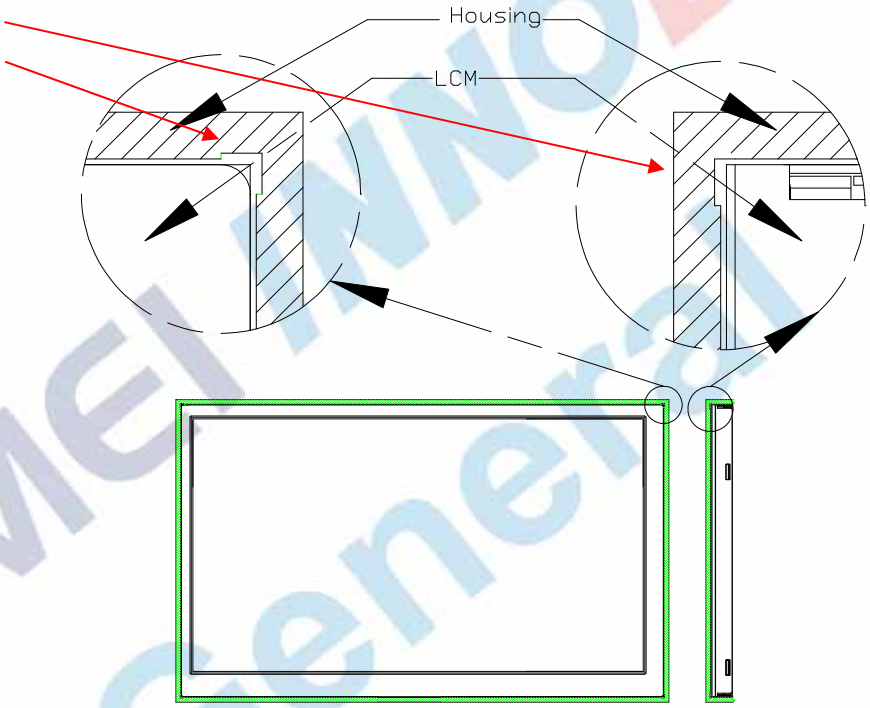
5.3 Vendor Recommend

Item	Vendor	Type	Remark
LED Driver	Fiti Power	FP6745	PWM Frequency:100Hz~50KHz

6. Suggestions For Housing Design

6.1 LCM corner /edge avoidable cutting.

If you design a avoidable cutting as the right drawing. LCM will easier to assemble in the housing.
When you use the LCM with TSP, the cutting will avoid damage the edge or corner of TSP during the assembly.

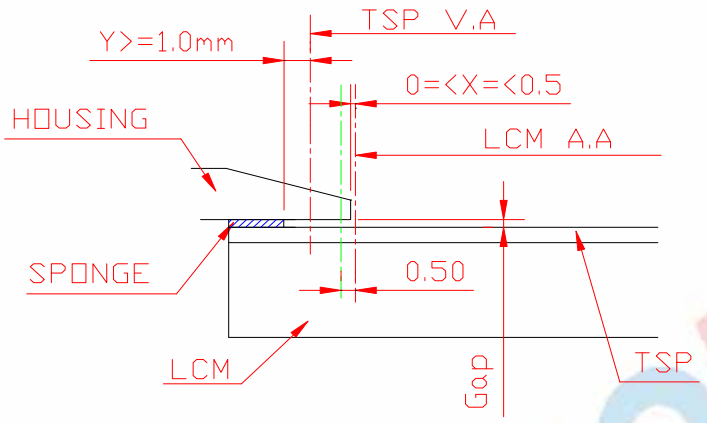


Suggestions of housing design

6.2 Housing opening design guide.

6.2.1 With TSP

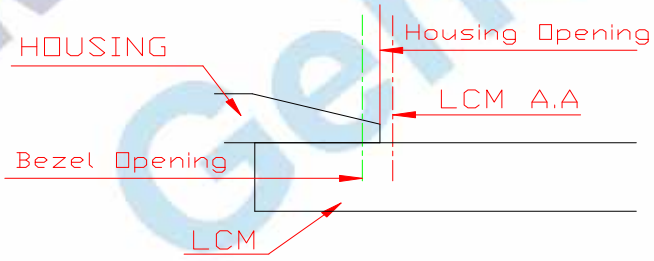
Because touch film is made of flexible PET, any unexpected touch with it would cause malfunction of touch panel. So here a sponge between touch panel and plastic housing is recommended for users. And the drawing will show you how to design the housing and sponge.



Section sketch (with TSP)

Notes: 1. X is the distance from LCM A.A to housing opening.
2. Y is the distance from TSP V.A to Sponge opening.
3. The active force will be bigger when you touch the area near the housing opening.
4. If you want to provide more protection for LCM, you can add same buffer material on the bottom of LCM.

6.2.2Without TSP



Section sketch(without TSP)

Notes: 1. Housing opening mast bigger than LCMA.A and cover the bezel .
2. If you want to provide more protection for LCM, you can add same buffer material on the top or bottom of LCM.

7. Demo Board Introduce

7.1 Interface of Demo Bard